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☐ 1. Document ID: KR 2000044929 A , KR 280809 B, US 6455366 B1

L1: Entry 1 of 1

File: DWPI

Jul 15, 2000

DERWENT-ACC-NO: 2001-179648
DERWENT-WEEK: 200307
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TITLE: Junction region formation in semiconductor device, involves performing implantation and thermal processes sequentially to form source and drain and elevated source and drain junctions

INVENTOR: LEE, J H

PATENT-ASSIGNEE:

ASSIGNEE

HYUNDAI ELECTRONICS IND CO LTD

CODE

HYUNN

PRIORITY-DATA: 1998KR-0061432 (December 30, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2000044929 A	July 15, 2000		000	H01L021/334
KR 280809 B	March 2, 2001		000	H01L021/334
US 6455366 B1	September 24, 2002		006	H01L021/8239

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
KR2000044929A	December 30, 1998	1998KR-0061432	
KR 280809B	December 30, 1998	1998KR-0061432	
KR 280809B		KR2000044929	Previous Publ.
US 6455366B1	December 22, 1999	1999US-0468883	

INT-CL (IPC): H01 L 21/334; H01 L 21/8239

ABSTRACTED-PUB-NO: KR2000044929A

BASIC-ABSTRACT:

NOVELTY - A nitride film (41) and a doped epitaxial silicon layer (27) are formed over peripheral and cell areas of a substrate (21) respectively. A source/drain junction (38) is formed in the peripheral area by sequentially performing a source/drain implantation process and a thermal process, such that during the thermal process the dopants of the silicon layer diffuses to form an elevated source/drain junction (28) at the cell area.

USE - For forming a junction region in a semiconductor device.

ADVANTAGE - Since the elevated source/drain region is formed only in the cell area and the source/drain ion implantation process and thermal process are performed only in the peripheral area, the metal contamination is reduced and the suppressing of diffusion dopants is lowered. Integration degree of the semiconductor device is increased.

DESCRIPTION OF DRAWING(S) - The figures show the sectional views of the forming junction in semiconductor device.

Substrate 21

Doped epitaxial silicon layer 27

Elevated source/drain junction 28

Source/drain junction 38

Nitride film 41 2B, 2C, 2D/2

ABSTRACTED-PUB-NO:

US 6455366B

EQUIVALENT-ABSTRACTS:

NOVELTY - A nitride film (41) and a doped epitaxial silicon layer (27) are formed over peripheral and cell areas of a substrate (21) respectively. A source/drain junction (38) is formed in the peripheral area by sequentially performing a source/drain implantation process and a thermal process, such that during the thermal process the dopants of the silicon layer diffuses to form an elevated source/drain junction (28) at the cell area.

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Substrate 21

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Nitride film 41 2B, 2C, 2D/2

TITLE-TERMS: JUNCTION REGION FORMATION SEMICONDUCTOR DEVICE PERFORMANCE IMPLANT
THERMAL PROCESS SEQUENCE FORM SOURCE DRAIN ELEVATE SOURCE DRAIN JUNCTION

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C02B; L04-C16;

EPI-CODES: U11-C02J6; U11-C05F1; U11-C18A3;

SECONDARY-ACC-NO:

CPI Secondary Accession Numbers: C2003-015463

Non-CPI Secondary Accession Numbers: N2003-046436

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